REMARKS

Claims 1, 2, 5-8, and 19-21 are pending after this amendment adds new claims 19-21. Claims 7 and 8 are amended to depend from claims 1 and 2, respectively. The amendments and new claims do not add new matter. Reconsideration and allowance of the above-identified application is respectfully requested.

DISCUSSION OF THE REJECTIONS UNDER 35 USC § 112, FIRST PARAGRAPH

Claims 1, 2, and 5-8 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The claims allegedly contain subject matter that was not described in the specification in such a way as to reasonable convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. In particular, the Office Action alleges that the claims 1, 2, and 5-8 require that the insulating layer formed directly below the floating gate and the gate of the select transistor form a tunneling gate oxide, and that there is no discussion in the specification or drawings, wherein the insulating layer directly below the select transistor forms a tunneling gate oxide. These rejections are respectively traversed. As discussed in greater detail below, the Applicant believes the specification more than adequately discloses the subject matter of the claimed invention.

Concerning the §112, first paragraph rejection, the Applicant respectfully submits that the specification fully supports the amendments that have been made to claims 1, 2, and 7 (as well as the features present in previously presented claim 8) to include the feature of an insulating layer formed directly under said floating gate and said gate of said select field effect transistor and forming a tunneling gate oxide layer.

The MPEP provides that "[t]o satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed

invention." MPEP §2163(I). Further, "[t]he fundamental factual inquiry is whether the specification conveys with **reasonable clarity** to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed." MPEP §2163(I)(B) (emphasis added). Additional case law supports the quoted sections of the MPEP that an exact duplication of the amendments to the claims, or each and every claim feature itself, need not be present in the specification, but rather only that the test is whether one of ordinary skill in the art could ascertain that the inventor had possession of the claimed invention ("The specification need not describe the claimed invention in *ipsis verbis* to comply with the written description requirement," *Ex Parte Sorenson*, 3 USPQ 2d 1462, 1463 (PTO Bd. App. & Int. 1987); "The test for determining whether the specification provides an adequate written description of the claimed invention is whether the originally filed specification disclosure reasonably conveys to a person having ordinary skill that applicant had possession of the subject matter later claimed," *Sorenson*, supra; see also, *Ex Parte Harvey*, 3 USPQ2d 1626, 1627 (PTO Bd. App. & Int. 1987), *Heymes v. Takaya*, 6 USPQ2d 1448, 1452 (PTO Bd. App. & Int. 1988), *Ex Parte Raible*, 8 USPQ2d 1709, 1710 (PTO Bd App & Int 1988), and *Texas Instruments v. ITC*, 10 USPQ2d 1257, 1263 (Fed. Cir. 1989)).

The Examiner's attention is directed towards page 15 of the originally filed specification, lines 14-25 and Figs. 7B and 7C (as well as pages 16, lines 7-10):

> [n]ext, as shown in Fig. 7B, the surface of the P-type silicon substrate is thermally oxidized at about 800 to 900°C, **whereby a tunnel gate oxide film 5 with the thickness of about 100 Angstroms is formed in a region that is to be an active region**. Further, **a polysilicon film 6 is stacked on the tunnel gate oxide film 5** by using a low pressure CVD (chemical vapor deposition) method. The film thickness of the polysilicon film 6 is about 1000 to 2000 Angstroms, for example, **and is to be a portion of a floating gate of the memory cell transistor MTr and a gate of the select transistor STr** in accordance with the subsequent steps.

Specification, page 15, lines 14-25 (emphasis added).

The Office Action asserts that "[t]here is no discussion in the specification or drawings, wherein the insulating layer directly below the select transistor forms a tunneling gate oxide. The Specification discloses a final structure having a first insulating layer directly below the floating gate, which forms a tunneling oxide, and a second insulating layer directly below the select gate, which forms a gate insulator." Clearly, however, support for the amendments to claims 1, 2, and 7, and the language of previously presented claim 8 is supported by the above cited section of the originally filed specification. The polysilicon film 6 is given as but one exemplary embodiment of a material that can be used to fabricate a portion of the floating gate of the memory cell transistor and the gate of the select transistor. The tunnel gate oxide film is directly below this film, as described in the claims and the specification. Consequently, it is respectively submitted that the specification conveys with reasonable clarity to skilled artisans that the Applicant was in possession of the invention as claimed on the filing date.

In view of the above, the Applicant respectfully requests the rejection of claims 1, 2, and 5-8 under 35 U.S.C. §112, first paragraph be withdrawn.

DISCUSSION OF THE REJECTIONS UNDER 35 § USC 102(b)

Claim 1 is rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 4,907,198 (hereinafter the "Arima Patent"). Claims 2 and 5-8 are presumed to have been likewise rejected, although the Office Action is silent with respect to those claims and a rejection under 35 U.S.C. §102(b). Specifically, the Applicant respectfully submits that the Arima Patent fails to teach or suggest the specific features of the embodiments of the present invention for a non-volatile semiconductor storage apparatus

and manufacturing method thereof as explicitly recited in independent claims 1, 2, 7, and 8.

In particular, the Applicant submits that the Arima Patent fails to disclose or suggest all of the features recited in independent claims 1, 2, 7, and 8, including the feature of an insulating layer formed directly below said floating gate and said gate of said select field effect transistor and forming a tunneling gate oxide layer in a region to be an active region of said unit cell.

Turning now to the §102 rejection, the Arima patent discloses an EEPROM formed of three-layer polysilicon. A floating gate is at a second level and a portion thereof is at a first level. A first control gate and a select gate are formed spaced apart from each other at the first level, and a portion of the second floating gate extends between them for formation of a tunnel region. A second control gate that is kept at the same potential as the first control gate exists at a third level. In the Amari EEPROM, electrons are drawn from the floating gate by applying a high voltage to the select gate.

The Office Action cites the Arima Patent, Figs. 8, and 10A-10I as disclosing, among others, the features of claim 1 of "a select field effect transistor having a diffused region (8) connected to a diffused region (8) of the memory cell field effect transistor," and "an insulating layer (21,6;) [sic] formed directly below the floating gate and the select gate, wherein the portion under the floating gate is used as a tunneling gate oxide in a region to be an active region of the unit cell."

In regard to the first claim feature, the Office Action alleges that the Arima Patent discloses "a select field effect transistor having a diffused region (8) connected to a diffused region (8) of the memory cell field effect transistor." The Office Action further states that:

> Arima teaches that the **diffusion layer (8) is used as a source for the select transistor and the field effect transistor, as opposed to being a drain for the select transistor and source for the memory cell field effect transistor**. However, this is a suggested use limitation, since the source/drain is a matter of how and where potential is applied. Accordingly, the requirement of the region being used as a drain for the select transistor connected to a source of the memory field effect transistor is not given any patentable weight, since it does not distinguish the structure of the claimed invention from the prior art.

Office Action, page 4 (emphasis added).

Respectfully, the Applicant disagrees with the conclusions stated in the Office Action. Specifically, the Applicant respectfully disagrees that the Applicant's claim features are a suggested use limitation. The Applicant also respectfully disagrees that the features of Applicant's claimed invention are not to be given any patentable weight. Furthermore, the Applicant respectfully disagrees that that the Applicant's invention is not structurally different from that of the cited prior art.

It is well known that "[a] claim is anticipated **only if each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 1053 (Fed. Cir. 1987) (emphasis added). It is fundamental that no limitations can be omitted in a rejection under 35 U.S.C. §102(b). Respectfully, the Applicant submits that the Arima Patent does not disclose a select field effect transistor having a drain connected to a source of said memory cell, and notes that the Office Action acknowledges the same.

The Arima Patent discloses, as shown in Figs. 7A-7C, a "semiconductor device memory device that comprises a floating gate transistor TR1 and a select transistor TR2,

formed on a main surface of a semiconductor substrate 11." Arima, Col. 7, lines 9-12. The floating gate transistor of the Arima Patent includes a source and drain regions 8 and 9. The select transistor TR2 comprises a source region 8, and a drain region 12. Furthermore, as the Office action acknowledges, "the impurity diffused layer 9 is the source of region of the floating gate transistor TR1 and also the source region of the selective transistor TR2 . . ." The Arima Patent, Col. 7, lines 32-34. Respectfully, this is not what is claimed in claim 1 of the Applicant's invention. In claim 1, "a select field effect transistor [has] a **drain connected to a source** of said memory cell." In the Arima Patent, the **source** of the selective transistor TR2 is connected to the **source** of the floating gate transistor TR1. This is a significant structural difference. Since the Arima patent does not disclose each and every claim feature of the Applicant's invention, the Arima Patent cannot anticipate it, and the Applicant respectfully suggests that the rejection under 35 U.S.C. 102(b) be withdrawn.

Further, the Office Action states that the "Arima teaches that the diffusion layer (8) is used as a source for the select transistor and the field effect transistor, as opposed to being a drain for the select transistor and source for the memory cell field effect transistor. However, this is **a suggested use limitation**, since the source/drain is a matter of how and where potential is applied." Office Action, page 4 (emphasis added). Respectfully, the Applicant does not know what the Office Action intends to convey by the term "suggested use limitation." There is no discussion in the Arima Patent, and the Office Action provides no suggestion there is, that this limitation is only "suggested" or that any other arrangement is an alternative contemplated in the Arima Patent. Also, the Office Action does not suggest or allude that the Applicant considers their arrangement to be merely suggestive as a "use limitation." The Office Action appears to be saying that the Applicant's invention can be anticipated by simply re-arranging the configuration of the selective and memory cell transistors' components of the Arima Patent. This argument fails for at least several different reasons. First, the Office Action cites no legal authority for such a conclusion. There is no case law, statutory law, rule or section of the

MPEP that stands for this proposition. Secondly, as is well known in the art, changing connections between drains and source of transistors provides a completely different device, that operates in a completely different manner. Third, there is a plethora of case law that states that each and every claim feature or limitation must be provided in a single prior document in order to anticipate the claimed invention. "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). It is incorrect for the Office Action to state that the Applicant's claim 1 features should be afforded "no patentable weight". Such a statement is inapposite to well settled law on the matter.

In regard to the second claim feature, the Office Action alleges the Arima Patent discloses, "an insulating layer (21,6;) [sic] formed directly below the floating gate and the select gate, wherein the portion under the floating gate is used as a tunneling gate oxide in a region to be an active region of the unit cell." Respectfully, the Applicant disagrees, and respectfully suggests that the Arima Patent does not disclose an insulating layer formed directly below said floating gate and said gate of said select field effect transistor and forming a tunneling gate oxide layer in an active region of said unit cell.

Attention is directed towards Figs. 7A-7C of the Arima Patent, as well as the following:

> The impurity diffused layer 8 is covered by the floating gate 2 in the plan view. The **tunnel region 14 is disposed so as to be completely covered with the floating gate 2**. The tunnel region 14 comprises a tunnel insulating film 6 formed on a main surface of the semiconductor substrate 11 and the impurity diffused layer 8. One end portion of the tunnel region 14 is defined by the select gate 3 and the first control gate 15. The other end portion of the tunnel region is defined so as to cross the select gate 3 and the first control gate 15 at right angles.

The Arima Patent, Col. 7, lines 40-17 (emphasis added).

Referring to Figs. 7A-7C, it can be seen that the tunnel region is defined by the extent of diffused layer 8, since the film 6 extends all over the substrate 11. As shown in Figs. 7A-7C, along with the portion of the Arima specification cited above, the tunnel region 14 cannot extend under both the floating gate and the select gate of TR2. The Arima Patent states that one end portion of the tunnel region 14 is defined by the select gate 3 and first control gate 15. In the first attachment, Fig. 7A, this is shown by lines A and B. The Arima Patent further states that "[t]he other end portion of the tunnel region 14 is defined so as to cross the select gate 3 and the first control gate 15 at right angles." First, note that Arima does not state that the tunnel region actually **crosses** the select gate 3 and control gate 15 at right angles; only that the tunnel region is defined "**so as to cross** the select gate". This is shown in attachments A and B as lines C and D. Because the Arima Patent clearly defines the tunnel region to be "formed on a main surface of the semiconductor substrate 11 and the impurity diffused layer 8," the tunnel region 14 does not actually cross either the select gate 3 or the first control gate 15. Instead, it is bound by the diffused layer 8, which is rectangular, and is shown by the darkened area in Attachment A. Furthermore, the Arima Patent clearly states (and Fig. 7A clearly shows) that the tunnel region 14 is disposed so as to be **completely covered** with the floating gate 2. The only area that satisfies all these requirements is the rectangular box 14 with the cross mark in it.

Therefore, the Applicant respectfully submits that the tunnel region 14 of the Arima Patent is not formed directly below said floating gate **and** said gate of said select field effect transistor. Since every feature of claim 1 has not been disclosed or suggested by the Arima Patent, the Arima Patent cannot anticipate claim 1 of the present invention, and it is respectfully requested that this rejection be withdrawn.

For all of the reasons discussed above with respect to the Arima Patent, the Applicant respectfully submits that the Arima patent does not anticipate claims 1, 2, and 5-8.

DISCUSSION OF NEW CLAIMS 19-21

New claim 19 depends from claim 1 and is therefore allowable for at least the same reasons as claim 1 is allowable. Additionally, claim 19 includes the feature that a common region forms the source of the memory cell field effect transistor and the drain of the select field effect transistor is defined by a tunnel insulating film of the memory cell field effect transistor and a gate insulating film of the select field effect transistor. It is respectfully submitted that none of the cited references disclose this additional feature, and therefore for this additional reason new claim 19 is allowable.

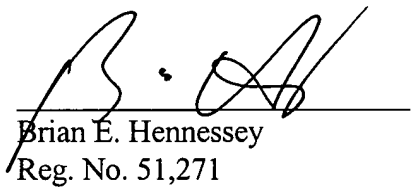
New claim 20 depends from claim 2 and is therefore allowable for at least the same reasons as claim 2 is allowable. Additionally, claim 20 includes the same feature discussed above in regard to claim 19. Since none of the cited references disclose this feature, new claim 20 is allowable.

New claim 21 is independent and relates to a non-volatile memory that includes, *inter alia*, a common diffusion layer formed on a third region of said semiconductor. The non-volatile memory of claim 21 is distinguishable from Arima in that the common diffusion layer formed on the third region defined by the gate insulating film (first region) and the tunnel insulating film (second region) is shared by the select transistor and the memory transistor. In the structure of Arima, the gate insulating film directly below the select transistor TR2 is provided adjacent to the tunnel insulating film 6 directly below the floating gate (see FIG. 7B). The common diffusion layer provided in the region defined by the gate insulating film and the tunnel insulating film does not exist, and thus, the structure is totally different. Therefore, claim 21 is allowable.

CONCLUSION

In view of the above, it is believed that the application is in condition for allowance and notice to this effect is respectfully requested. Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the telephone number indicated below.

Respectfully submitted,



Brian E. Hennessey
Reg. No. 51,271

Katten, Muchin Rosenman
575 Madison Avenue
New York, NY 10022-2585
Telephone: (212)940-8800
Facsimile: (202) 940-8986/7